BOLYMIN

SPECIFICATIONS FOR
OLED MODULE

RoHS
COMPLIANT

MODEL NO.
BL1602A1ERNBU$
VER.01

FOR MESSRS:

ON DATE OF:

APPROVED BY:

BOLYMIN, INC.
5F, No. 38, Keya Rd., Daya Dist., Central Taiwan Science Park, Taichung City, 42881, Taiwan.
Web Site:http://www.bolymin.com.tw TEL:+886-4-25658689 FAX:+886-4-25658698

History of Version

Version	Contents	Date	Note
01	NEW VERSION	2017/07/28	SPEC.

CONTENTS

1. Numbering System

B	L	1602	A1	E	R	N	B	U	$
0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	L=PLED/OLED	
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A1 type	
4	LCD Color	L=OLED/Green W=OLED/White K= OLED/Blue	E=OLED/Yellow R=OLED/Red
5	LCD Type	R=positive/reflective	
6	Backlight type/color	N=No backlight	
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font B= English/Japanese/European	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	U=Bottom/Ultra wide Temperature	
9	Special Code	n=positive voltage for LCD	$=RoHS

2.General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of Characters	16 characters ×2 Lines	dots
Panel dimension (L*W*H)	68.5 x 17.5 x 2.0	mm
View area	58.22 x 13.52	mm
Active area	56.22 x 11.52	mm
Dot size	0.57 x 0.67	mm
Dot pitch	0.60 x 0.70	mm
Character size (L x W)	2.97 x 5.57	mm
Character pitch (L x W)	3.55 x 5.95	mm

(2) Controller IC: US2066 Controller

3. Absolute Maximum Ratings

Item	Symbol	Condition	Min	Max	Unit
Operating Temperature	TOP		-40	+85	℃
Storage Temperature	TST		-40	+90	℃
Supply Voltage(Logic)	VDD		-0.3	6.0	V
Input Voltage	VI		GND-0.3	VDD+0.3	V
Operating life time		150 cd/m²	50000	—	Hrs
Operating life time		120 cd/m²	80000		Hrs

Note:(A) Under VCC = 12V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(C) Lifetime should be counted once shipping out from our warehouse . But the exact lifetime must depend on customer's operation enviornment and application.

※ Software configuration follows Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

4.Electrical Characteristics

(Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (VDDIO)	VDDIO	—	4.5	5.0	5.5	V
Supply Voltage (VCC)	VCC		11.5	12.0	12.5	V
Input High Vol	V_{IH}	—	$0.8V_{DD}$	—	V_{DD}	V
Input Low Vol	V_{IL}	—	0	—	$0.2V_{DD}$	V
Output High Vol	V_{OH}	—	$0.9V_{DD}$	—	—	V
Output Low Vol.	V_{OL}	—	—	—	$0.1V_{DD}$	V
Supply Current(Yellow)	IDD	—	—	33	40	mA

※VDD= 5.0V, VCC = 12.0V, 100% Display Area Turn on. Display color= Yellow .

5. Optical Characteristics

Item	Min.	Typ.	Max.	Unit
View Angle	Free	—	—	deg
Dark Room contrast	—	>10000:1	—	—
Pixel Luminance	120	150		cd/m2
CIE x,y (Color: Yellow)	(0.46,0.45)	(0.50,0.49)	(0.54,0.53)	

6.Interface Pin Function

<table>
<tr><th>Pin No</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>1</td><td>NC</td><td>-</td><td>-</td></tr>
<tr><td>2</td><td>VSL</td><td>P</td><td>This is segment voltage reference pin.
When external V_{SL} is not used, this pin should be left open.
When external V_{SL} is used, this pin should connect with resistor and diode to ground.</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>REGVDD</td><td>I</td><td>This is internal V_{DD} regulator selection pin in 5V I/O application mode.
When this pin is pulled “Low”, internal V_{DD} regulator is disabled. (Low Voltage I/O Application)
When this pin is pulled “High”, internal V_{DD} regulator is enabled.</td></tr>
<tr><td>5</td><td>SHLC</td><td>I</td><td>This pin is used to determine COM output scanning direction. It can still be programmable and defined by fundamental command.</td></tr>
<tr><td>6</td><td>SHLS</td><td>I</td><td>This pin is used to change the mapping between the display data column address and the segment driver. It can still be programmable and defined by fundamental command.</td></tr>
<tr><td>7</td><td>VDD</td><td>P</td><td>This is a voltage supply pin which is supplied externally or regulated internally. A capacitor should be connected between this pin and V_{SS} under all circumstances. When internal V_{DD} is disabled, this is a power input pin. It must be connected to V_{DDIO} or external source and always be equal to or lower than V_{DDIO}. (Low Voltage I/O Application) When internal V_{DD} is enabled, it is regulated internally from V_{DDIO}.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>This is a voltage supply pin. It should match with the MCU interface voltage level and must be connected to external source</td></tr>
<tr><td>9</td><td>BS0</td><td rowspan="3">I</td><td rowspan="3">These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I^2C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Serial</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>4-bit 68XX Parallel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>4-bit 80XX Parallel</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>10</td><td>BS1</td></tr>
<tr><td>11</td><td>BS2</td></tr>
<tr><td>12</td><td>GPIO</td><td>I/O</td><td>This pin could be left open individually or have signal inputted/ outputted. It is able to use as the external DC/DC converter circuit enabled/disabled control or other applications.</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. When serial interface mode is selected, this pin must be connected to V_{SS}. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
</table>

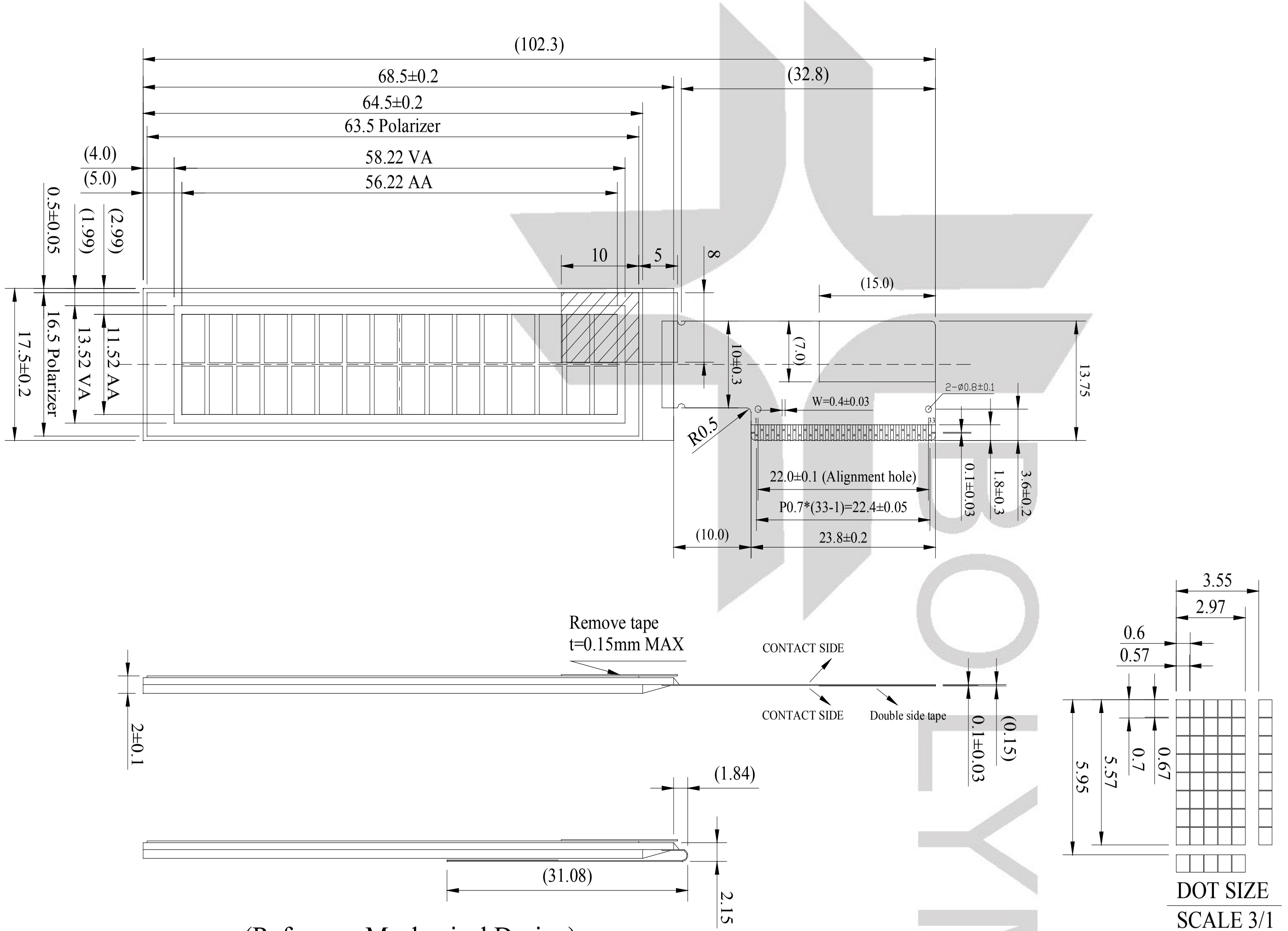
<table>
<tr><td>16</td><td>R/W#</td><td>I</td><td>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I 2 C mode is selected, this pin must be connected to V SS .</td></tr>
<tr><td>17</td><td>E/RD#</td><td>I</td><td>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
When serial or I 2 C mode is selected, this pin must be connected toV_{SS} .</td></tr>
<tr><td>18</td><td>D0</td><td rowspan="8">I/O</td><td rowspan="8">These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D0 will be the serial clock input SCLK; D1 will be the serial data input SID and D2 will be the serial clock output SOD. When I ^{2} C mode is selected, D2, D1 should be tired together and serve as SDA $_{OUT}$, SDA IN in application and D0 is the serial clock input, SCL. Unused pins must be connected to V_{SS} except.</td></tr>
<tr><td>19</td><td>D1</td></tr>
<tr><td>20</td><td>D2</td></tr>
<tr><td>21</td><td>D3</td></tr>
<tr><td>22</td><td>D4</td></tr>
<tr><td>23</td><td>D5</td></tr>
<tr><td>24</td><td>D6</td></tr>
<tr><td>25</td><td>D7</td></tr>
<tr><td>26</td><td>IREF</td><td>I</td><td>This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS} . Set the current at 15μA.</td></tr>
<tr><td>27</td><td>ROM0</td><td rowspan="2">I</td><td rowspan="2">These pins are used to select the appropriate character ROM. See the following table :
<table>
<tr><td></td><td>ROM0</td><td>ROM1</td></tr>
<tr><td>ROM A</td><td>0</td><td>0</td></tr>
<tr><td>ROM B</td><td>1</td><td>0</td></tr>
<tr><td>ROMC</td><td>0</td><td>1</td></tr>
</table>
It can still be programmable and defined by extended command.</td></tr>
<tr><td>28</td><td>ROM1</td></tr>
<tr><td>29</td><td>OPR0</td><td rowspan="2">I</td><td rowspan="2">These pins are used to manage the character number of character generator. See the following table:
<table>
<tr><td>CGROM</td><td>CGRAM</td><td>OPR0</td><td>OPR1</td></tr>
<tr><td>240</td><td>8</td><td>0</td><td>0</td></tr>
<tr><td>248</td><td>8</td><td>1</td><td>0</td></tr>
<tr><td>250</td><td>6</td><td>0</td><td>1</td></tr>
<tr><td>256</td><td>0</td><td>1</td><td>1</td></tr>
</table>
It can still be programmable and defined by extended command.</td></tr>
<tr><td>30</td><td>OPR1</td></tr>
<tr><td>31</td><td>VCOMH</td><td>P</td><td>This pin is the input pin for the voltage output high level for COM signals.A capacitor should be connected between this pin and V SS .</td></tr>
<tr><td>32</td><td>VCC</td><td>P</td><td>This is the most positive voltage supply pin of the chip. It must be connected to external source.</td></tr>
<tr><td>33</td><td>NC</td><td>-</td><td>-</td></tr>
</table>

MCU interface assignment under different bus interface mode

Pin Name Interface	Data/Command interface								Control Signal		
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E	R/W	RS
6800,8-bit	DB[7:0]								E	R/W	RS
8080,8-bit	DB[7:0]								/RD	/WR	RS
SPI	Tied LOW					SOD	SID	SCLK	Tied LOW		
I2C	Tied LOW					SDO	SDA	SCL	Tied LOW		SA0

7. Drawing & Block Diagram

7.1 Drawing



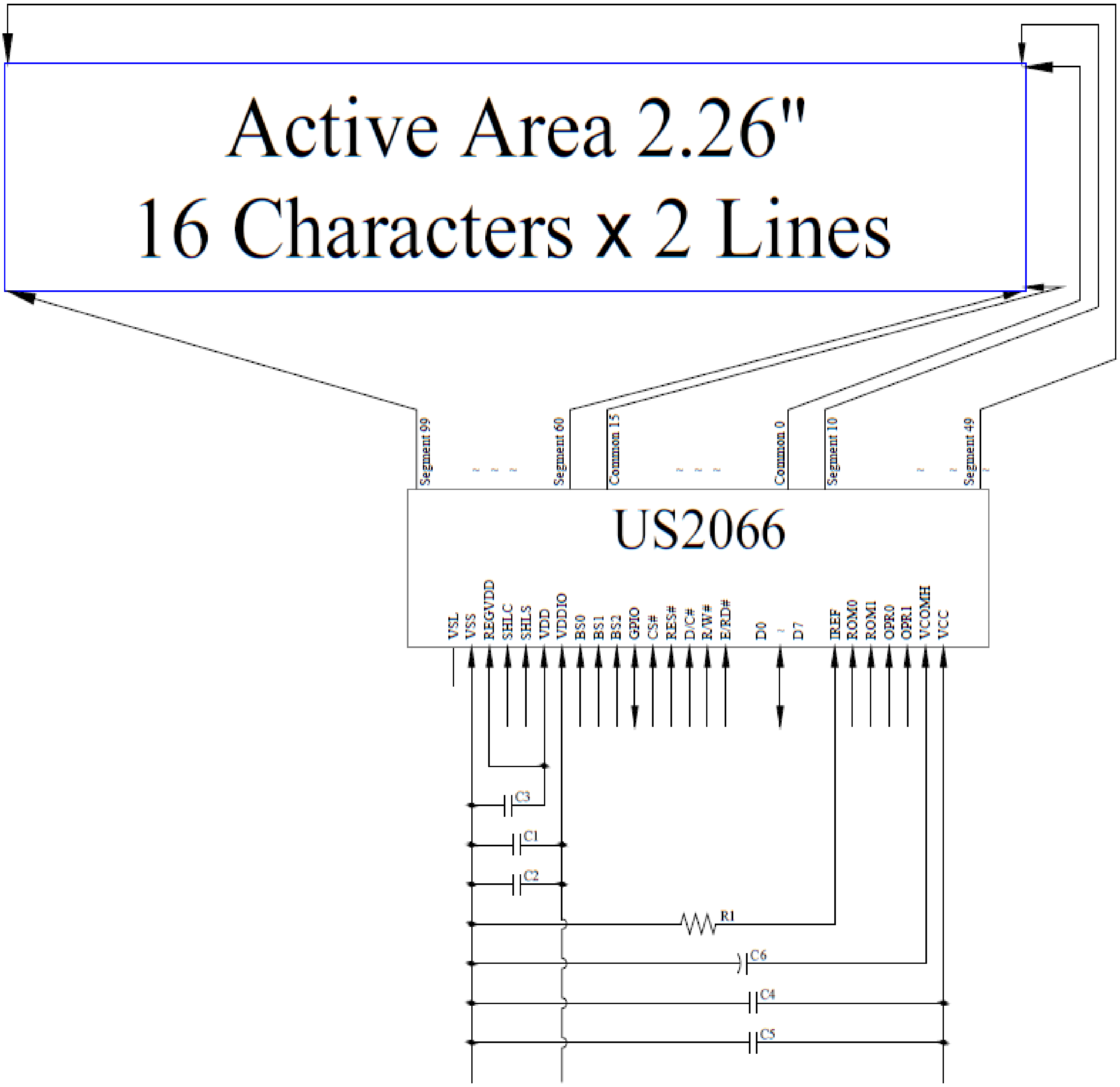
(Reference Mechanical Design)

PIN NO.	SYMBOL
1	NC
2	VSL
3	VSS
4	REGVDD
5	SHLC
6	SHLS
7	VDD
8	VDDIO
9	BS0
10	BS1
11	BS2
12	GPIO
13	#CS
14	#RES
15	D/C
16	R/W(#WR)
17	E(#RD)
18	D0
19	D1
20	D2
21	D3
22	D4
23	D5
24	D6
25	D7
26	IREF
27	ROM0
28	ROM1
29	OPR0
30	OPR1
31	VCOMH
32	VCC
33	NC

NOTE:
1.THE NON-SPECIFIED TOLERANCE OF DIMENSION IS ±0.3mm
2.PANEL TYPE:OLED,
3.DRIVE IC : US2066
4.OPERATING TEMP : -40 ℃ ~ +85 ℃
5.STORAGE TEMP : -40 ℃ ~ +90 ℃
6.CONNECTION : FPC

SCALE: 1/1	REV: 00	寶麗明股份有限公司 BOLYMIN,INC.
UNIT: mm	PAGE: 1/1	MODEL BL1602A1W
APPROVE		TITLE LCM DRAWING
CHECK		DWG NO.
DRAW	Allen 2013.11.05	

7.2 BLOCK DIAGRAM



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7
* SHLC, SHLC, ROM0, ROM1, OPR0 and OPR1 should be configured.

C1, C4: 0.1μF
C2: 4.7μF
C3: 1μF
C5: 10μF
C6: 4.7μF / 25V Tantalum Capacitor
R1: 470kΩ, R1 = (Voltage at IREF - VSS) / IREF

8.US2066 Controller Data

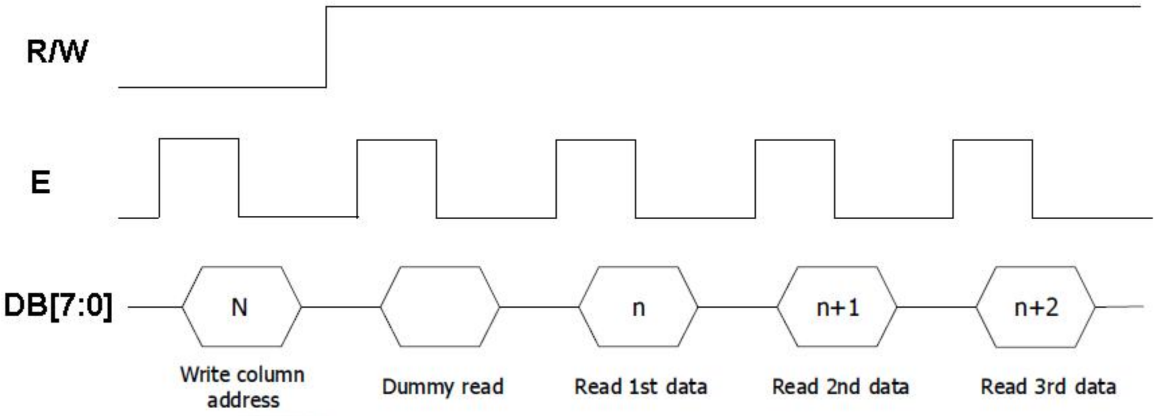
8.1 MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (DB[7:0]), R/W, RS, E.
A LOW in R/W indicates WRITE operation and HIGH in R/W indicates READ operation.
A LOW in RS indicates COMMAND read/write and HIGH in RS indicates DATA read/write.
The E input serves as data latch signal. Data is latched at the falling edge of E signal.

Function	**E**	**R/W**	**RS**
Write command	↓	L	L
Read status	↓	H	L
Write data	↓	L	H
Read data	↓	H	H

Control pins of 6800 interface

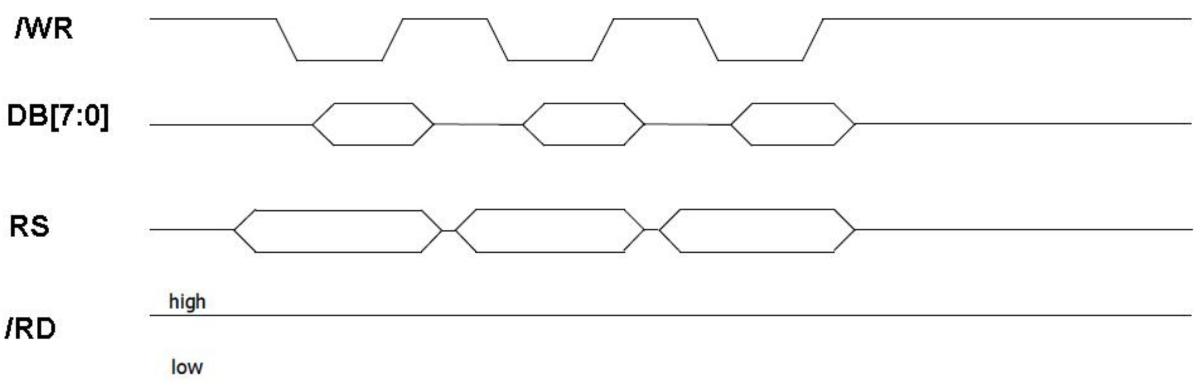
In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read.



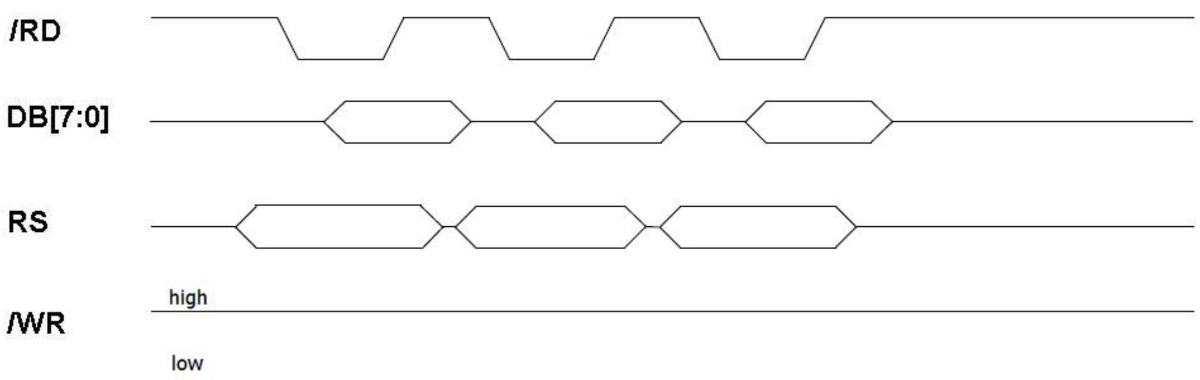
Data read back procedure - insertion of dummy read

8.2 MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (DB[7:0]), /RD ,/WR, RS.
A LOW in RS indicates COMMAND read/write and HIGH in RS indicates DATA read/write.
A rising edge of /RD input serves as a data READ latch signal.
A rising edge of /WR input serves as a data/command WRITE latch signal.

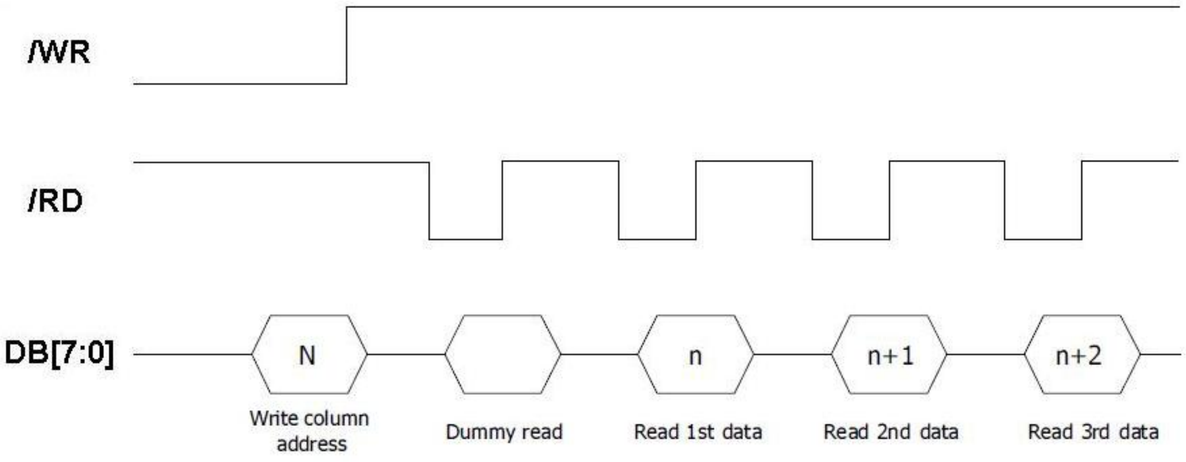


Example of Write procedure in 8080 parallel interface mode



Example of Read procedure in 8080 parallel interface mode

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown below.

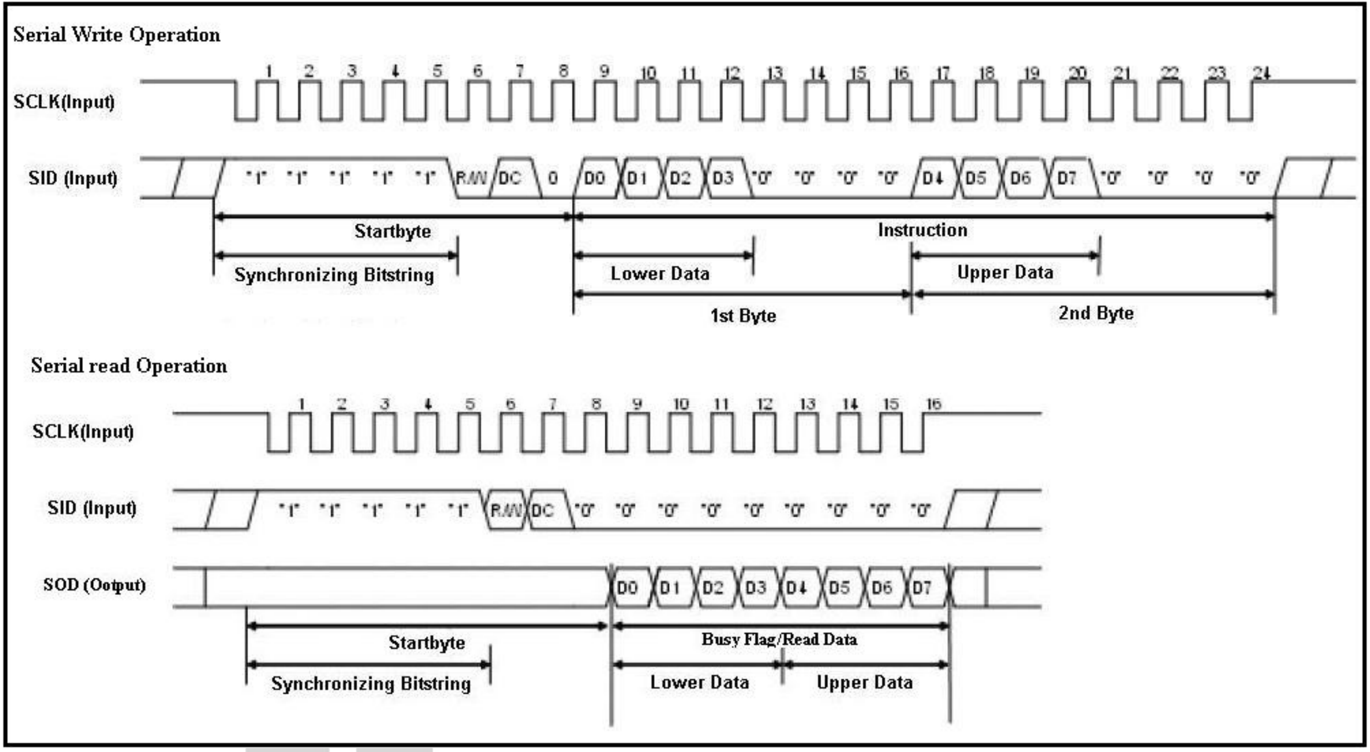


8.3 Serial Interface

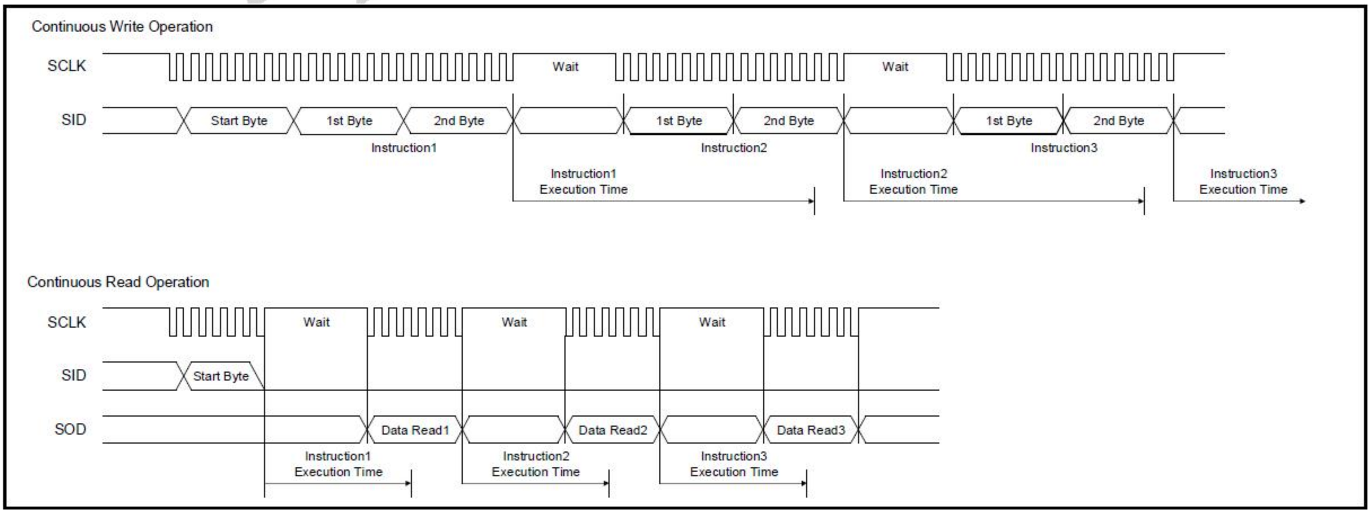
When serial interface mode (SPI) is started, all the three ports, SCLK(DB0), SID(DB1) and SOD(DB2) are used. Before transfer real data, start byte has to be transferred. It is composed of succeeding five "High" bits, read write control bit (R/W), register selection bit (RS) and end bit that indicates the end of start byte. Whenever succeeding five "High" bits are detected by US2066, it makes serial transfer counter reset and ready to receive next information.

The next input data are register selection bit that determine which register will be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (Refer to the two Figures below).

8.3.1 Timing Diagram



Timing Diagram of Serial Data Transfer



Timing Diagram of Continuous Data Transfer

8.4 MCU I2C Interface

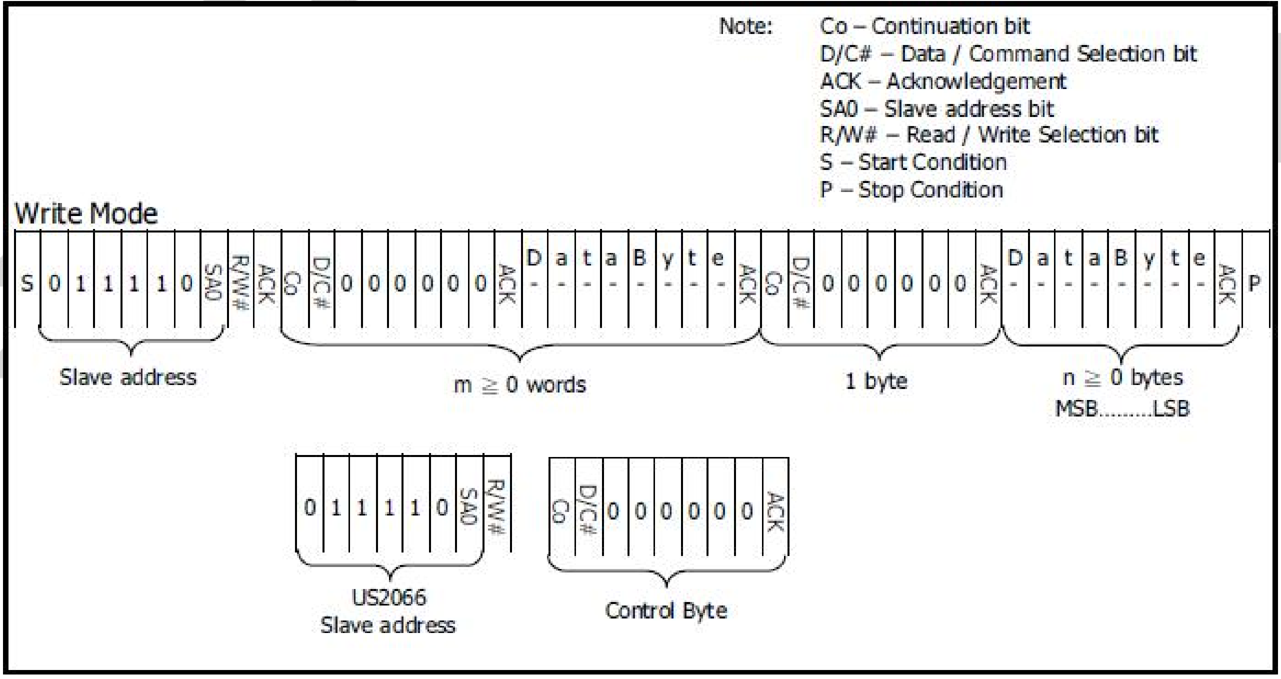
The I2C communication interface consists of slave address bit SA0, I2C-bus data signal SDA (SDAOUT/DB2 for output and SDAIN/DB1 for input) and I2C-bus lock signal SCL (DB0). BL2004AW has to recognize the slave address before transmitting or receiving any information by the I2C-bus.The device will respond to the slave address following by the slave address bit (“SA0” bit) and the read/write select bit (“R/W#” bit) with the following byte format,

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	1	1	0	SA0	R/W

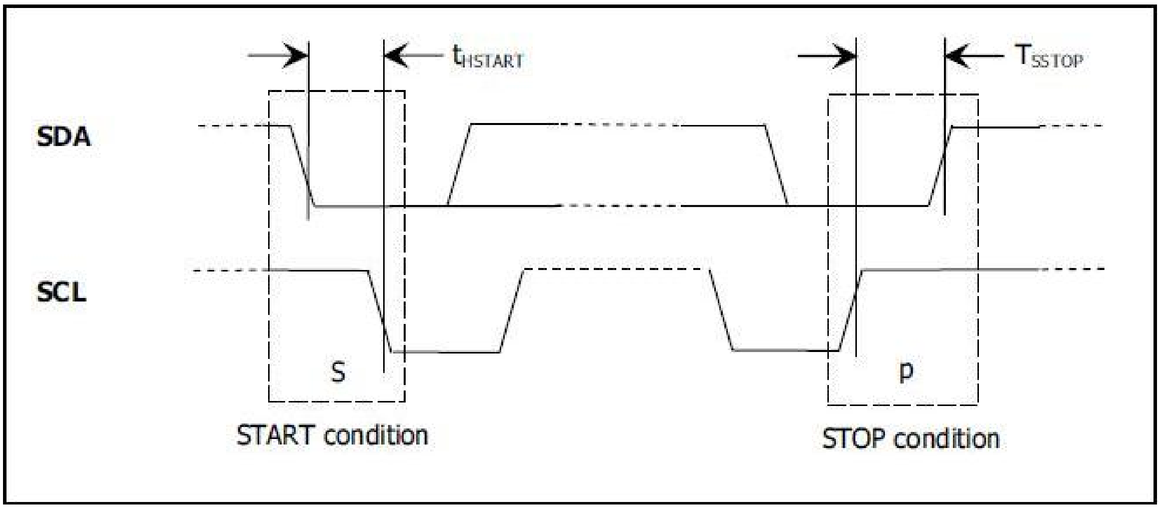
“SA0” bit provides an extension bit for the slave address. Either “0111100” or “0111101” can be selected as the Slave address of BL2004AWLRNEHn20c.RS pin acts as SA0 for slave address selection.
R/W bit is used to determine the operation mode of the I2C-bus interface.
R/W=1, it is in read mode.
R/W=0, it is in write mode.

I2C-bus Write data

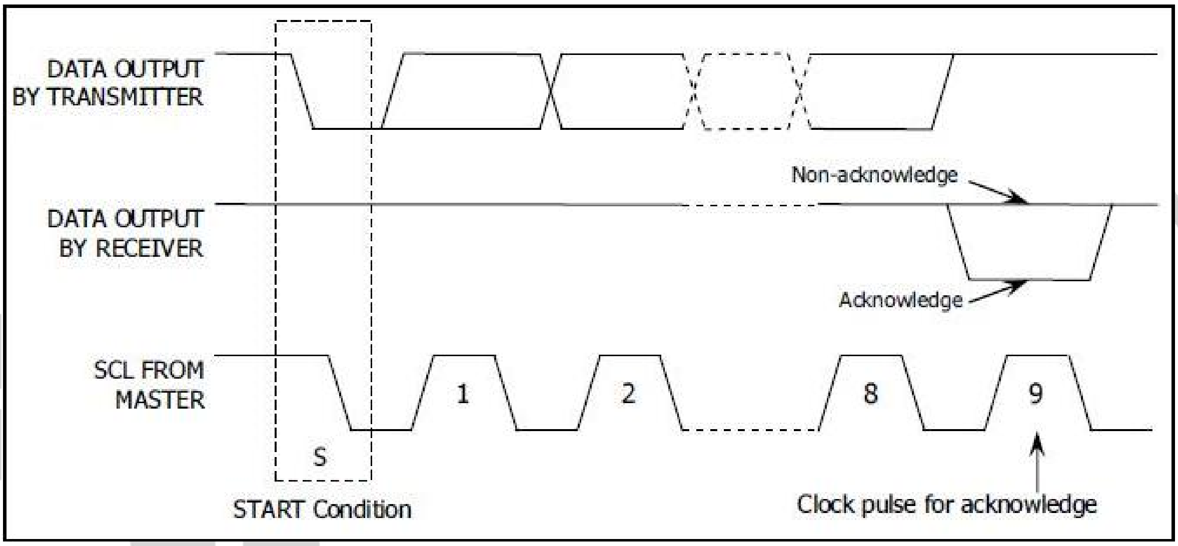
Please refer to Figure below for the write mode of I2C bus in chronological order.



I2C-bus data format

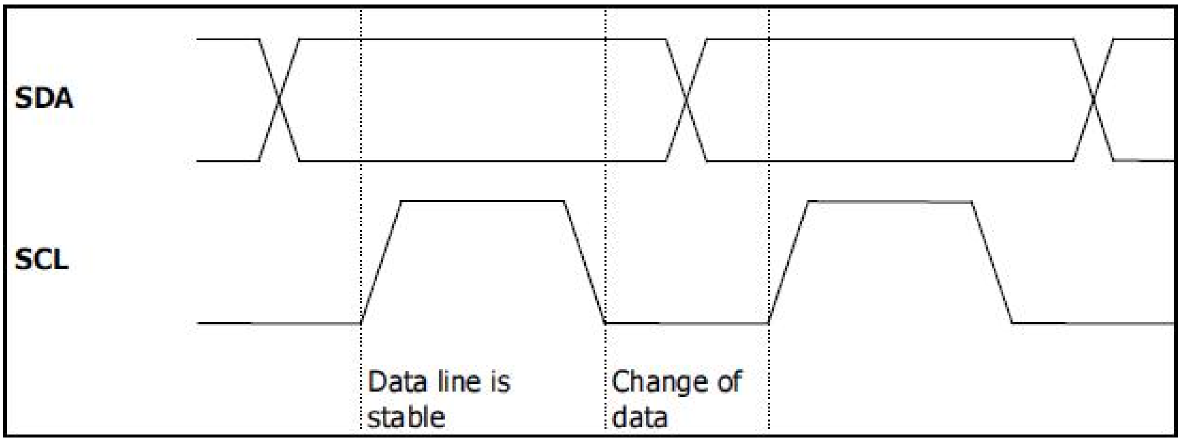


Definition of the Start and Stop Condition



Definition of the acknowledgement condition

The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure below for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.

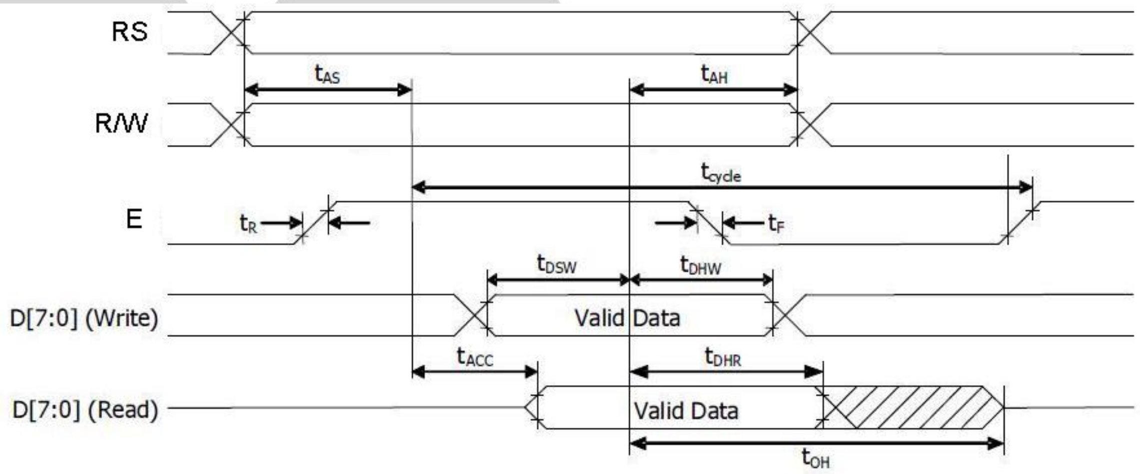


Definition of the data transfer condition

8.5 Timing Characteristics

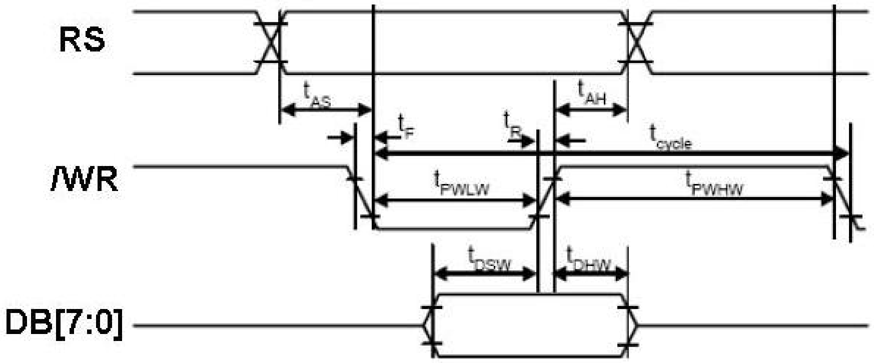
6800 MPU Interface

Symbol	Parameter	Min	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	ns
t_{AS}	Address Setup Time	13	-	ns
t_{AH}	Address Hold Time	17	-	ns
t_{CS}	Chip Select Time	0	-	ns
t_{CH}	Chip Select Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	35	-	ns
t_{DHW}	Write Data Hold Time	18	-	ns
t_{DHR}	Read Data Hold Time	13	-	ns
t_{OH}	Output Disable Time	10	90	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	125	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) Chip Select Low Pulse Width (read Command) Chip Select Low Pulse Width (write)	250 250 50	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	155 55	- -	ns ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

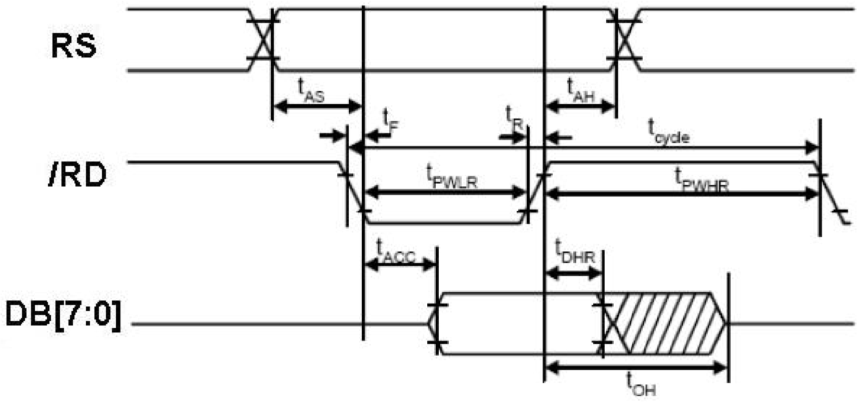


8080 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	400	-	-	ns
t_{AS}	Address Setup Time	13	-	-	ns
t_{AH}	Address Hold Time	17	-	-	ns
t_{CS}	Chip Select Time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	0	-	-	ns
t_{DSW}	Write Data Setup Time	35	-	-	ns
t_{DHW}	Write Data Hold Time	18	-	-	ns
t_{DHR}	Read Data Hold Time	13	-	-	ns
t_{OH}	Output Disable Time	10	-	70	ns
t_{ACC}	Access Time (RAM) Access Time (command)	-	-	125	ns ns
PW_{CSL}	Chip Select Low Pulse Width (read RAM) - t_{PWLR} Chip Select Low Pulse Width (read Command) - t_{PWLR} Chip Select Low Pulse Width (write) - t_{PWLW}	250 250 50	- - -	- - -	ns ns ns
PW_{CSH}	Chip Select High Pulse Width (read) - t_{PWHR} Chip Select High Pulse Width (write) - t_{PWHW}	155 55	- -	- -	ns ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



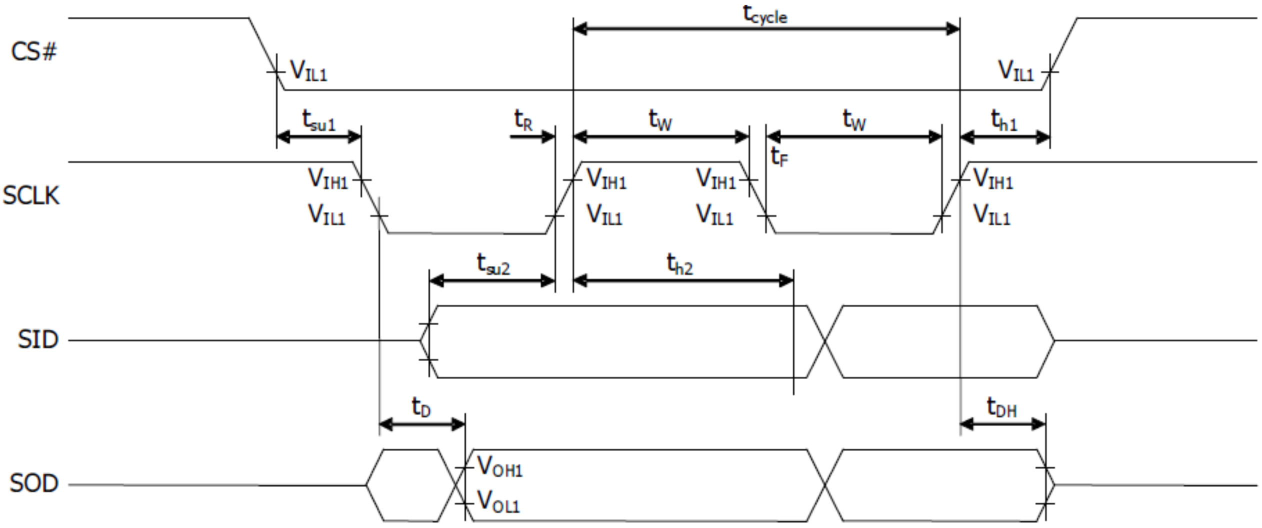
Write Cycle



Read Cycle

SPI MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_c	Serial clock cycle time	1	-	20	us
t_r, t_f	Serial clock rise/fall time	-	-	15	ns
t_w	Serial clock width (high, low)	400	-	-	ns
t_{su1}	Chip select setup time	60	-	-	ns
t_{h1}	Chip select hold time	20	-	-	ns
t_{su2}	Serial input data setup time	200	-	-	ns
t_{h2}	Serial input data hold time	TBD	-	-	ns
t_D	Serial output data delay time	-	-	TBD	ns
t_{DH}	Serial output data hold time	10	-	-	ns

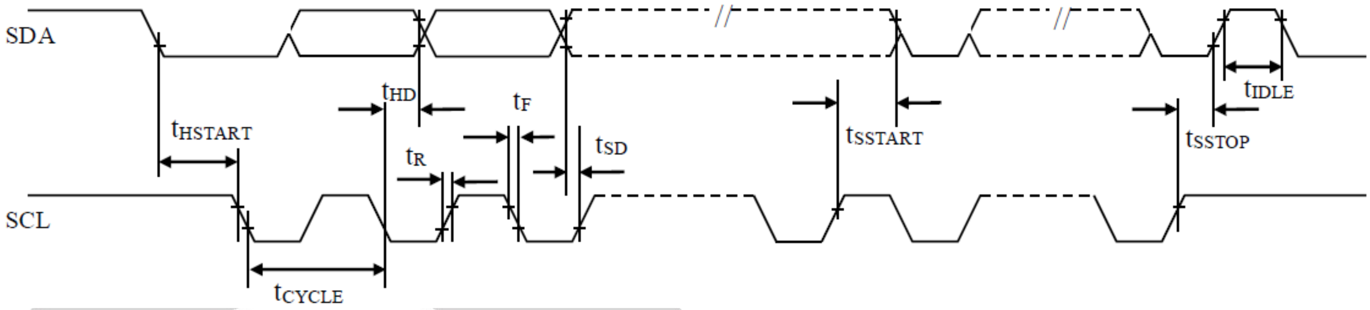


Serial Timing Characteristics

***: CS# in Serial Timing Characteristics always tied to GND.

I2C MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	5	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



8.6 Display Control Instruction

There are three sets of command set in US2066: Fundamental Command Set, Extended Command Set and OLED Command Set. These three command sets can be selected by setting logic bits IS, RE and SD accordingly.

1. Fundamental Command Set												
Command	IS/ RE /SD	Instruction code										Description
		D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Clear Display	X /X /0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC.
Return Home	X/ 0/ 0	0	0	0	0	0	0	0	0	1	*	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.
Entry Mode Set	X /0/ 0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR)
	X/ 1/ 0	0	0	0	0	0	0	0	1	BDC	BDS	Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99
Display ON /OFF Control	X /0 /0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR).
Extended Function Set	X /1/ 0	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR), B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable (POR) NW = "1": 3-line or 4-line display mode NW = "0": 1-line or 2-line display mode

1. Fundamental Command Set

Command	IS/ RE /SD	Instruction code										Description
		D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Cursor or Display Shift	0/ 0/ 0	0	0	0	0	0	1	S/C	R/L	*	*	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left
Double Height (4-line) / Display-dot shift	0/ 1/ 0	0	0	0	0	0	1	UD2	UD1	*	DH’	UD2~1: Assign different doubt height format (POR=11b). DH’ = "1": display shift enable DH’ = "0": dot scroll enable (POR)
Shift Enable	1/ 1/ 0	0	0	0	0	0	1	DS4	DS3	DS2	DS1	DS[4:1]=1111b (POR) when DH’ = 1b Determine the line for display shift. DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.
Scroll Enable	1/1/0	0	0	0	0	0	1	HS4	HS3	HS2	HS1	HS[4:1]=1111b (POR) when DH’ = 0b Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.
Function Set	X/0/0	0	0	0	0	1	*	N	DH	RE (0)	IS	Numbers of display line, N when N = "1": 2-line (NW=0b) / 4-line (NW=1b), when N = "0": 1-line (NW=0b) / 3-line (NW=1b) DH = “ 1/0”: Double height font control for2-line mode enable/ disable (POR=0) Extension register, RE ("0") Extension register, IS
	X/1/0	0	0	0	0	1	*	N	BE	RE (1)	REV	CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Extension register, RE ("1") Reverse bit REV = "1": reverse display, REV = "0": normal display (POR)

Notes
(1) POR stands for Power on Reset Values.
(2) “*” and “X” stand for “Don’t care”.

1. Fundamental Command Set												
Command	IS/ RE /SD	Instruction code										Description
		D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
Set GRAM address	0/0/0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.(POR=00 0000)
Set DRAM Address	X/0/0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.(POR=000 0000)
Set Scroll Quantity	X/1/0	0	0	1	*	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Set the quantity of horizontal dot scroll.(POR=00 0000) Valid up to SQ[5:0] = 110000b
Read Busy Flag and Address/ Part ID	X/X/0	0	1	BF	AC6/ ID6	AC5/ ID5	AC4/ ID4	AC3/ ID3	AC2/ ID2	AC1/ ID1	AC0/ ID0	Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state
Write data	X/X/0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM).
Read data	X/X/0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM).

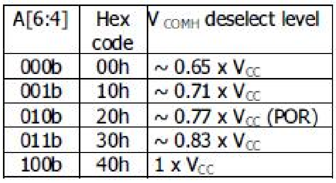
Notes
(1) POR stands for Power on Reset Values.
(2) “*” and “X” stand for “Don’t care”.

<table>
<tr><th colspan="13">2. Extended Command Set</th></tr>
<tr><th rowspan="2">Command</th><th rowspan="2">IS/ RE /SD</th><th colspan="10">Instruction code</th><th rowspan="2">Description</th></tr>
<tr><th>D/C</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Function Selection A</td><td>X/1/0
X/1/0</td><td>0
1</td><td>0
0</td><td>0
A7</td><td>1
A6</td><td>1
A5</td><td>1
A4</td><td>0
A3</td><td>0
A2</td><td>0
A1</td><td>1
A0</td><td>A[7:0] = 00h, Disable internal V_{DD} regulator at 5V I/O application mode.

A[7:0] = 5Ch, Enable internal V_{DD} regulator at 5V I/O application mode (POR)</td></tr>
<tr><td>Function Selection B</td><td>X/1/0
X/1/0</td><td>0
1</td><td>0
0</td><td>0
*</td><td>1
*</td><td>1
*</td><td>1
*</td><td>0
ROM1</td><td>0
ROM0</td><td>1
OPR1</td><td>0
OPR0</td><td>OPR[1:0]: Select the character no. of character generator
<table>
<tr><th>OPR[1:0]</th><th>CGROM</th><th>CGRAM</th></tr>
<tr><td>00b</td><td>240</td><td>8</td></tr>
<tr><td>01b</td><td>248</td><td>8</td></tr>
<tr><td>10b</td><td>250</td><td>6</td></tr>
<tr><td>11b</td><td>256</td><td>0</td></tr>
</table>
ROM[1:0]: Select character ROM
<table>
<tr><th>RO[1:0]</th><th>ROM</th></tr>
<tr><td>00b</td><td>A</td></tr>
<tr><td>01b</td><td>B</td></tr>
<tr><td>10b</td><td>C</td></tr>
<tr><td>11b</td><td>Invalid</td></tr>
</table></td></tr>
<tr><td>OLED Characterization</td><td>X/1/X</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>SD</td><td>Extension register, SD
SD = 0b: OLED command set is disabled (POR)
SD = 1b: OLED command set is enabled</td></tr>
</table>

Notes
(1) POR stands for Power on Reset Values.
(2) “*” and “X” stand for “Don’t care”.

3. OLED Command Set

Command	IS/ RE /SD	D/C	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
Set Contrast Control	X/1/1 X/1/1	0 0	0 0	1 A7	0 A6	0 A5	0 A4	0 A3	0 A2	0 A1	1 A0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh)
Set Display Clock Divide Ratio/ Oscillator Frequency	X/1/1 X/1/1	0 0	0 0	1 A7	1 A6	0 A5	1 A4	0 A3	1 A2	0 A1	1 A0	A[3:0]: Define the divide ratio (D) of the display clocks (DCLK): divide ratio = A[3:0] + 1 (POR=0000b) A[7:4]: Set the Oscillator Frequency, Fosc. Oscillator Frequency increases with the value of A[7:4] and vice versa. (POR=0111b) Range:0000b~1111b Frequency increases as setting value increases.
Set Phase Length	X/1/1 X/1/1	0 0	0 0	1 A7	1 A6	0 A5	1 A4	1 A3	0 A2	0 A1	1 A0	A[3:0]: Phase 1 period of up to 32 DCLK; clock 0 is an valid entry with 2 DCLK (POR=1000b) A[7:4]: Phase 2 period of up to 15 DCLK; clock 0 is invalid entry (POR=0111b)
Set SEG Pins Hardware Configuration	X/1/1 X/1/1	0 0	0 0	1 A7	1 A6	0 A5	1 A4	1 A3	0 A2	1 A1	0 A0	A[4]=0b, Sequential SEG pin configuration A[4]=1b (POR),Alternative (odd/even) SEG pin configuration A[5]=0b (POR), Disable SEG Left/Right remap. A[5]=1b, Enable SEG Left/Right remap
Set V_{COMH} Deselect Level	X/1/1 X/1/1	0 0	0 0	1 0	1 A6	0 A5	1 A4	1 0	0 0	1 0	1 0	

A[6:4]	Hex code	V_{COMH} deselect level
000b	00h	~ 0.65 x V_{CC}
001b	10h	~ 0.71 x V_{CC}
010b	20h	~ 0.77 x V_{CC} (POR)
011b	30h	~ 0.83 x V_{CC}
100b	40h	1 x V_{CC}

Notes
(1) POR stands for Power on Reset Values.
(2) “*” and “X” stand for “Don’t care”.

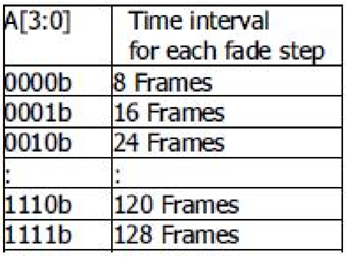
<table>
<tr><th colspan="13">3. OLED Command Set</th></tr>
<tr><th rowspan="2">Command</th><th rowspan="2">IS/ RE /SD</th><th colspan="10">Instruction code</th><th rowspan="2">Description</th></tr>
<tr><th>D/C</th><th>R/W</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Function Selection C</td><td>X/1/1
X/1/1</td><td>0
0</td><td>0
0</td><td>1
A7</td><td>1
0</td><td>0
0</td><td>1
0</td><td>1
0</td><td>1
0</td><td>0
A1</td><td>0
A0</td><td>Set VSL & GPIO

Set VSL:
A[7] = 0b: Internal VSL (POR)
A[7] = 1b: Enable external VSL.

Set GPIO:
A[1:0]= 00b represents GPIO pin HiZ, input disabled (always read as low)
A[1:0]= 01b represents GPIO pin HiZ, input enabled
A[1:0]= 10b represents GPIO pin output Low (RESET)
A[1:0]= 11b represents GPIO pin output High.</td></tr>
<tr><td>Set Fade Out and Blinking</td><td>X/1/1
X/1/1</td><td>0
0</td><td>0
0</td><td>0
*</td><td>0
*</td><td>1
A5</td><td>0
A4</td><td>0
A3</td><td>0
A2</td><td>1
A1</td><td>1
A0</td><td>A[5:4] = 00b Disable Fade Out /Blinking Mode[RESET]

A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled.

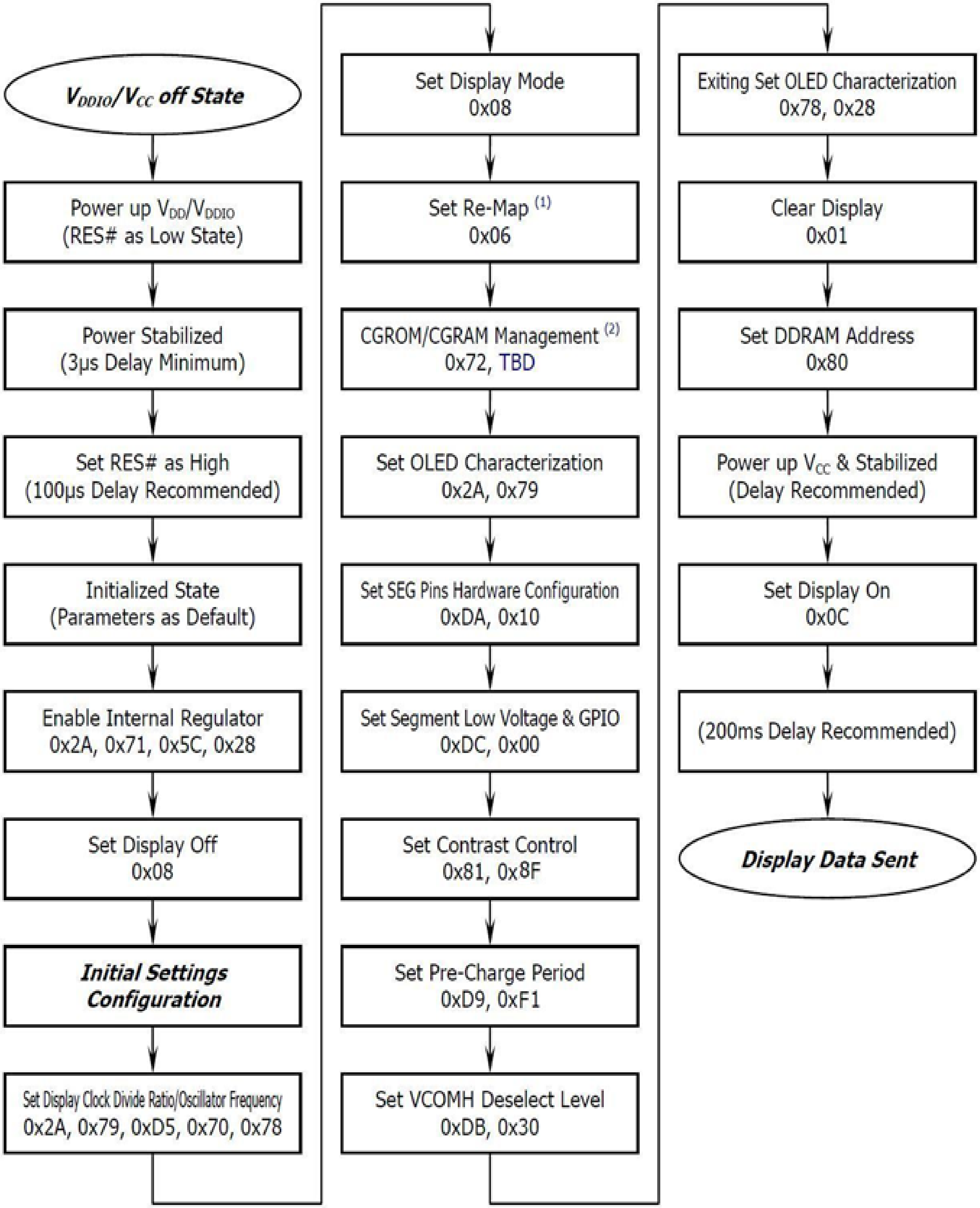
A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled.

A[3:0] : Set time interval for each fade
Step

<table>
<tr><th>A[3:0]</th><th>Time interval for each fade step</th></tr>
<tr><td>0000b</td><td>8 Frames</td></tr>
<tr><td>0001b</td><td>16 Frames</td></tr>
<tr><td>0010b</td><td>24 Frames</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>1110b</td><td>120 Frames</td></tr>
<tr><td>1111b</td><td>128 Frames</td></tr>
</table></td></tr>
</table>

Notes
(1) POR stands for Power on Reset Values.
(2) “*” and “X” stand for “Don’t care”.
(3) Detail command description, please refer to IC Spec.: US2066

8.7 I/O Application

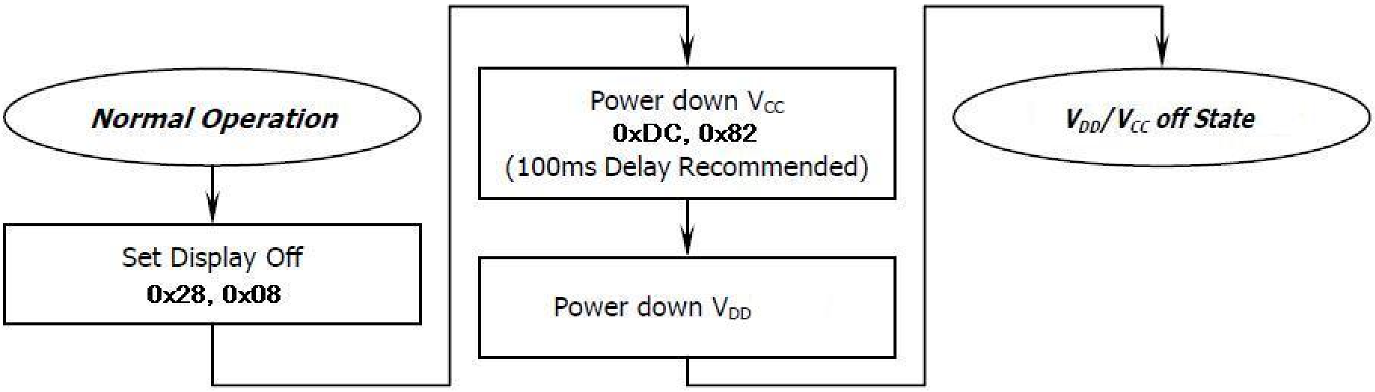
8.7.1 Power up sequence



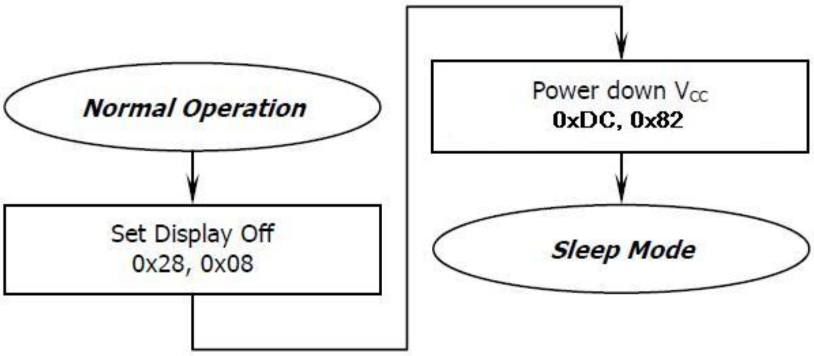
Recommended Power up sequence

```
void initial(void)
{
comm_out(0x2a);//Function Set
comm_out(0x71);//Function Selection A
data_out(0x5c); //Enable internal VDD
comm_out(0x28);//Function Set

comm_out(0x08);//Display OFF Control
//--OLED Command Set------------------------------------
comm_out(0x2a);//Function Set
comm_out(0x79);//OLED Characterization
comm_out(0xd5);
comm_out(0x70);
comm_out(0x78);

comm_out(0x08);//Set Display Mode

comm_out(0x06);//Set Re-Map

comm_out(0x72);//CRGOM/CGRAM Management
data_out (0x00);//For reference

comm_out(0x2a);//Function Set
comm_out(0x79);//OLED Characterization

comm_out(0xda);//Set SEG Pins Hardware Configuration
comm_out(0x10);

comm_out(0xdc);//Function Selection C
comm_out(0x00);

comm_out(0x81);//Set Contrast Control
comm_out(0x8F);Depend on OLED color

comm_out(0xd9);//Set Phase Length
comm_out(0xf1);

comm_out(0xdb);//Set VCOMH Deselect Level
comm_out(0x30);

comm_out(0x78);//OLED Characterization
comm_out(0x28);//Function Set

comm_out(0x01);//Clear Display

comm_out(0x80);//Set DDRAM address

comm_out(0x0c);//Display ON Control

}
```

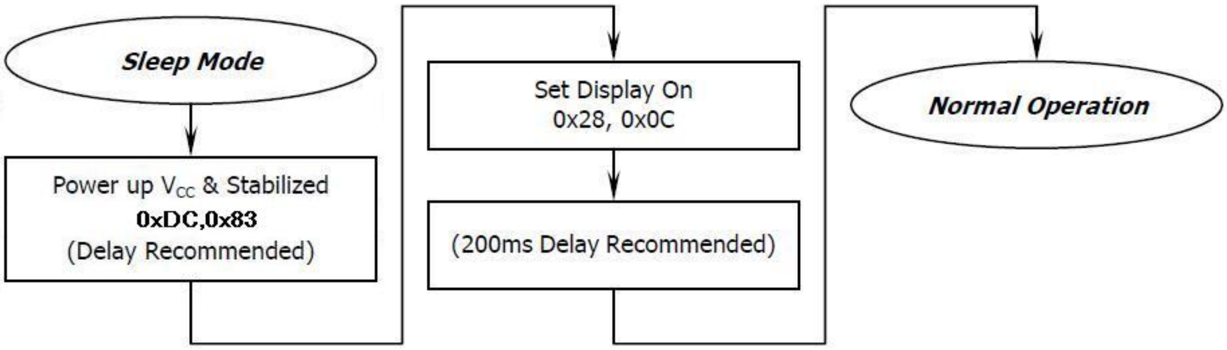
8.7.2 Power down sequence



8.7.3 Enter sleep mode



8.7.4 Exit sleep mode



9.CGROM& CGRAM

9.1 CGROM character code

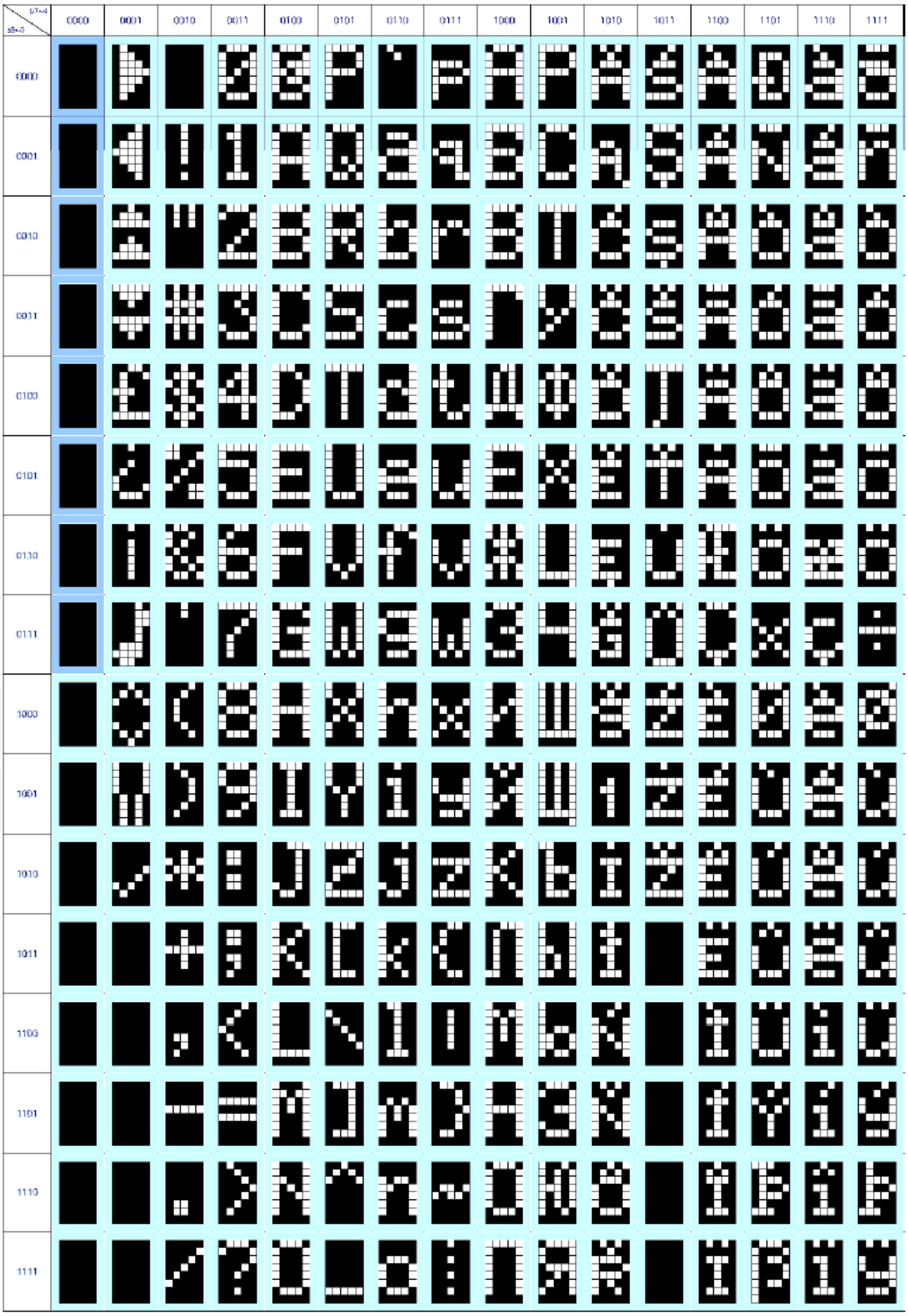
ROM A (ROM[1:0] = [0:0])

Language: English, Irish, Spanish, Dutch (2), Danish, Norwegian, Swedish, Finnish, Czech (7), Slovene, Hungarian (2), Turkish (1)

The number in the parentheses is showing how many letters might be needed to build and define additionally.

The darker background is showing the maximum addresses those could be allocated by OPR[1:0] setting.

ROM B (ROM[1:0] = [0:1])

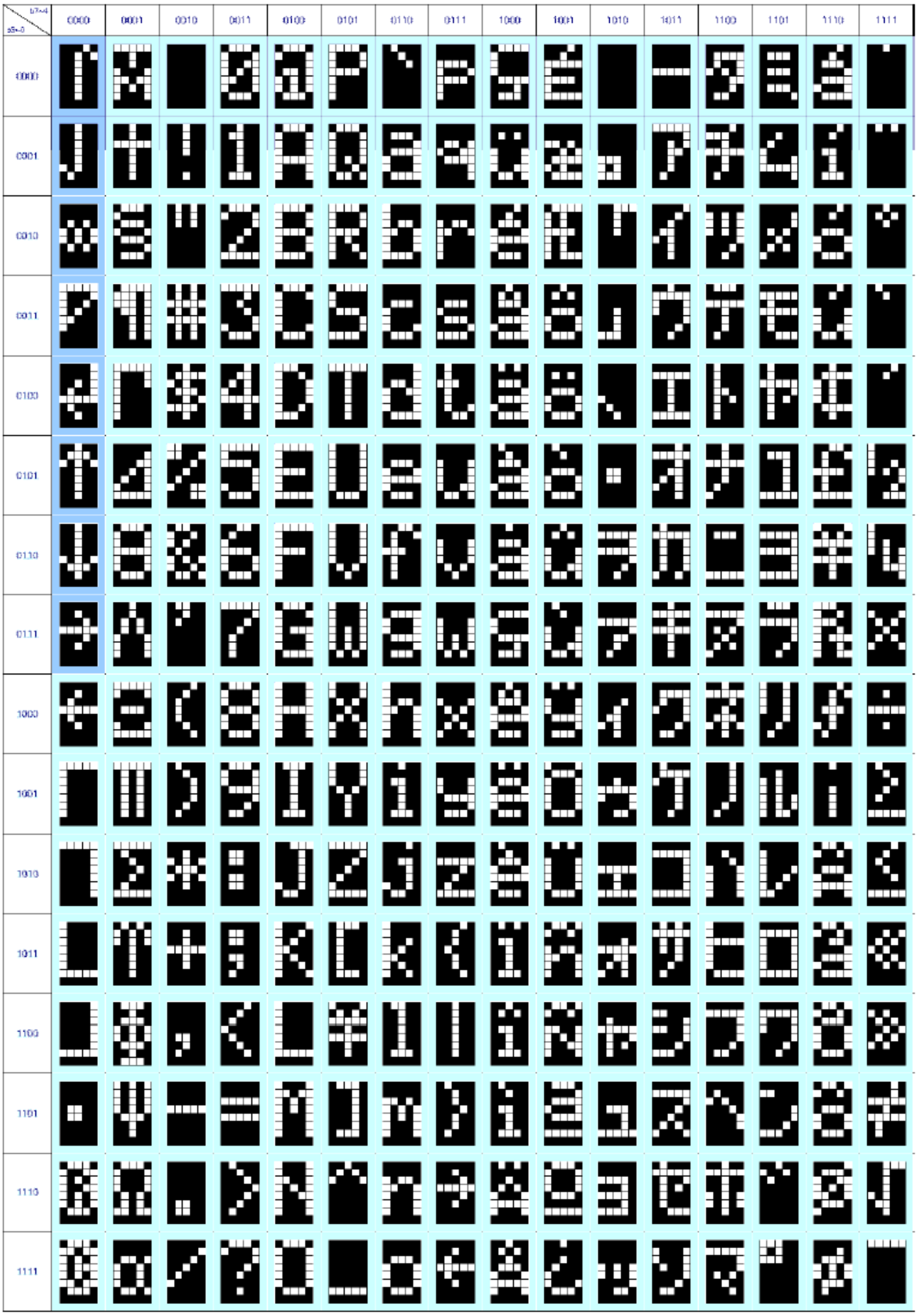


Language: English, Irish, Portuguese, Spanish, French (1), Italian, German, Dutch (2), Icelandic, Danish, Norwegian, Swedish, Polish (8),Czech (8), Hungarian (2), Romanian (5), Turkish, Vietnamese (6), Russian (Small Letters)

The number in the parentheses is showing how many letters might be needed to build and define additionally.

The darker background is showing the maximum addresses those could be allocated by OPR[1:0] setting.

ROM C (ROM[1:0] = [1:0])



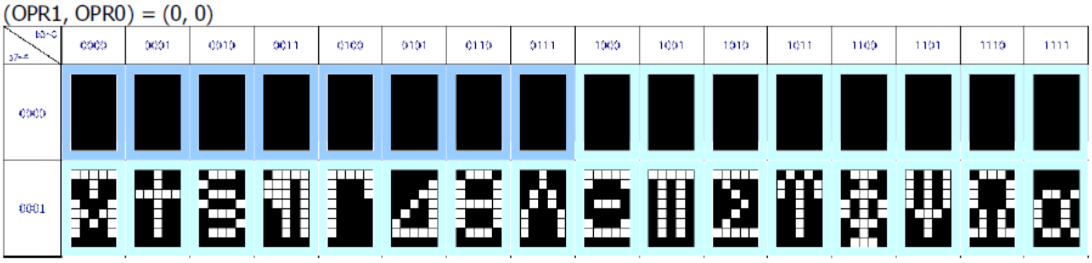
Language: English, Dutch (2), Japanese, Greek (Small Letters)

The number in the parentheses is showing how many letters might be needed to build and define additionally.

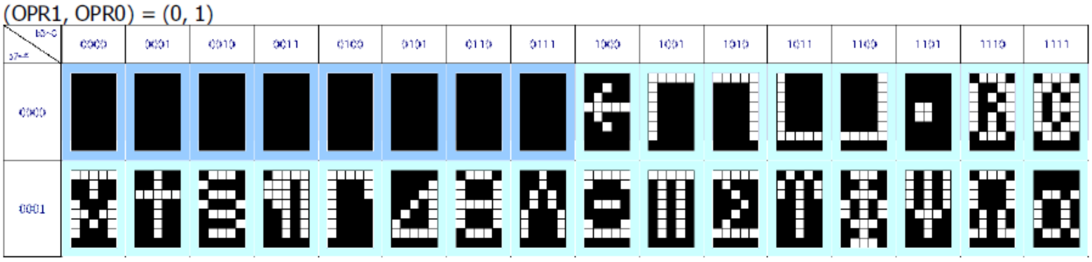
The darker background is showing the maximum addresses those could be allocated by OPR[1:0] setting.

9.2 CGRAM (Character Generator RAM)

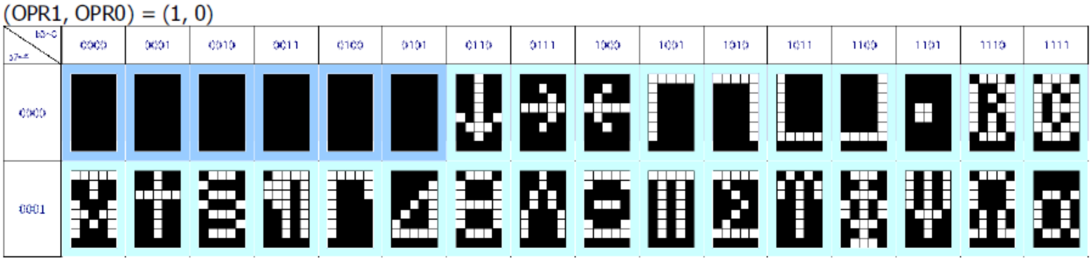
(OPR1, OPR0) = (0, 0)



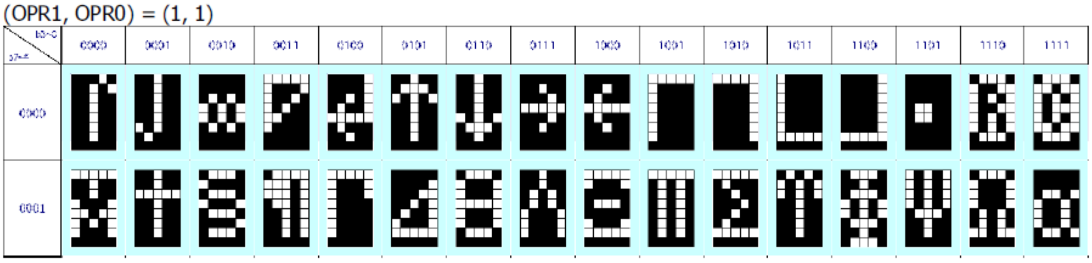
(OPR1, OPR0) = (0, 1)



(OPR1, OPR0) = (1, 0)



(OPR1, OPR0) = (1, 1)



10. Quality Assurance

10.1 Inspection conditions

1. The inspection and measurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector ≧30㎝

10.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm) W</th><th>Length (mm) L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.1</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>W>0.1</td><td>L≦2</td><td>n=1</td></tr>
<tr><td></td><td>L＞2</td><td>n=0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td><td></td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ ≦0.5</td><td>Ignore</td></tr>
<tr><td>Φ>0.5</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、Lighting spot、Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.25</td><td>1</td></tr>
<tr><td>0.25＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

Bolymin . Will provide one-year warranty for the products only if under specification operating conditions.

If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.

Bolymin would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 50K hours.

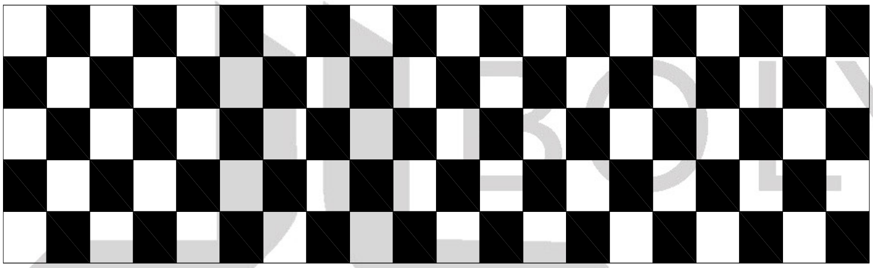
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: VCC=12.0V

10.4.2.2 Luminance: <150 cd/m^2.

10.4.2.3 Operation temperature and humidity :< 25℃ and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminance has decayed to less than 50% of the initial measured luminance.

11. Reliability

■Content of Reliability Test

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	90°C, 240hrs	——
2	High temp. (Operation)	85°C,240hrs	——
3	Low temp. (Non-Operation)	-40°C, 240hrs	——
4	Low temp. (Operation)	-40°C, 240hrs	——
5	High temp. / High. humidity (Operation)	60°C, 90%RH, 240hrs	——
6	Thermal shock(Non-operation)	-40°C ~85°C,100 cycles. 60 mins dwell	——

Test and measurement conditions
1. The degradation of Polarizes are ignored.
2. No moisture condensation is observed during tests.

Failure Check Standard
After the completion of the described reliability test, the samples were left at room temperature for 2hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

Criteria
1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption: within ±50% of initial value.

Reliability Test

Bolymin only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won’t produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don’t use the panels that were tested for subsequent tests.

12. Precautions for Handling

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the driver IC and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module.
    Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

13. Precautions for Electrical

13.1. Design using the settings in the specification

It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel mal-functioning.

13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.

The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is dvisable to store the packed cartons or packages at 23℃±5℃,55%±10%RH(Note A), Do not store the OLED module under direct sunlight or UV light and for best panel performance.The constant working OLED display module decays slower than the module that is not working. And it's better to use the module on the field within one month after unpacking the package.

Note (A):

Vacuum Packaging


Desiccant x 2


Humidity indicator card

Humidity indicator card

As the humidity increases, the chemically impregnated spots change from a brown color (DRY) to a blue color (HUMID).